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(71) Applicant: **Oki Electric Industry Co., Ltd.**
Tokyo (JP)

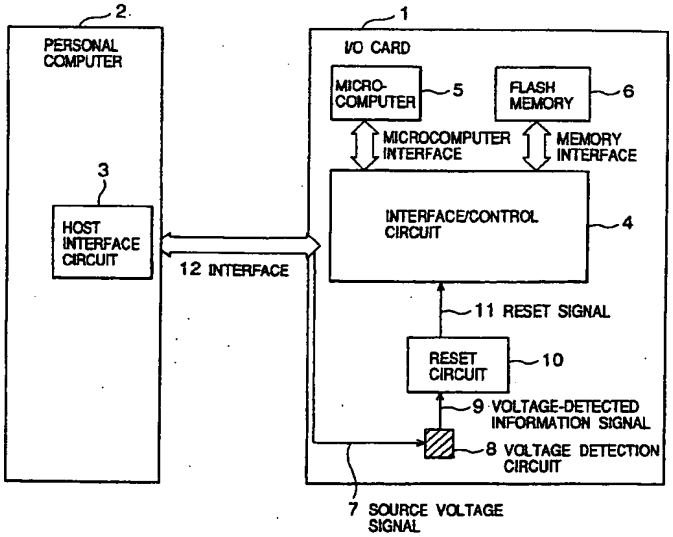
(72) Inventors:
- **Ohno, Yasuhiro,**
  c/o Oki Electric Ind. Co., Ltd
  Minato-ku, Tokyo (JP)
- **Unno, Yusaku,**
  c/o Oki Electric Ind. Co., Ltd
  Minato-ku, Tokyo (JP)

(74) Representative: **Betten & Resch**
Reichenbachstrasse 19
D-80469 München (DE)

(54) Internal state determining apparatus

(57) An internal state determining apparatus according to the present invention includes at least one inner circuit, means for detecting a change in voltage supplied from an external device and outputting a detected signal in response to the change in voltage and internal state determining means for determining the inner circuit so as to fall into a predetermined state in response to the detected signal, as components that make up the internal state determining apparatus. Owing to the internal state determining apparatus having such a construction, when an IC card is activated in response to two types of different voltages, for example, an internal state of the IC card can be reliably determined without burdening a host computer.

FIG.1



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Description

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to an internal state determining apparatus applicable to an IC memory card, an I/O (Input/Output) card or the like.

Description of the Related Art:

An IC card such as an IC memory card, an I/O card or the like, which is activated in response to two types of supply source voltage signals is now becoming pervasive. Standard specifications for this type of IC card have been fixed by the PCMCIA (PC Memory Card International Association) corresponding to the IC Memory Card Standard Association in the United States of America.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an internal state determining apparatus capable of determining an internal state of an IC memory card or an I/O card without burdening a host-side device during a period in which the host-side device supplies predetermined power to the IC memory card or the I/O card based on an initial supply voltage signal.

According to one aspect of the invention, for achieving the above object, there is provided an internal state determining apparatus comprising: at least one inner circuit; detecting means for detecting a change in voltage supplied from an external device and outputting a detected signal in response to the change in voltage; and internal state determining means for determining the inner circuit so as to fall into a predetermined state in response to the detected signal.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects, features and advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a functional configuration view of a personal-computer system showing a first embodiment;
Fig. 2 is a detailed circuit diagram of a reset circuit employed in the first embodiment shown in Fig. 1;
Fig. 3 is a waveform chart for describing the operation of the personal-computer system shown in Fig. 1;
Fig. 4 is a functional configuration view of a personal-computer system illustrating a second embodiment;
Fig. 5 is a functional configuration view of a select circuit employed in the second embodiment shown in Fig. 4;
Fig. 6 is a functional configuration view of an interface circuit employed in the second embodiment shown in Fig. 4;
Fig. 7 is a functional configuration view of a clock generation circuit employed in the second embodiment shown in Fig. 4; and
Fig. 8 is a waveform chart for describing the operation of the personal-computer system shown in Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments in which the present invention is applied to I/O cards used for personal-computer systems, will hereinafter be described with reference to the accompanying drawings.

[First embodiment]: [configuration of system]

Fig. 1 is a functional configuration view of a personal-computer system showing a first embodiment. Referring to Fig. 1, the present system principally comprises an I/O card 1 and a personal computer 2. An interface 12 electrically connects between the I/O card 1 and the personal computer 2.

Described specifically, the personal computer 2 includes a host interface circuit 3 for interfacing with the I/O card 1. On the other hand, the I/O card 1 is composed of an interface/control circuit 4, a microcomputer 5, a flash memory 6, a voltage detection circuit 8 and a reset circuit 10.

The I/O card 1 is characterized in configuration by the voltage detection circuit 8 and the reset circuit 10.

The interface/control circuit 4 and the host interface circuit 3 are electrically connected to each other by the interface 12. A source voltage signal 7 supplied to the interface/control circuit 4 from the host interface circuit 3 is applied to the voltage detection circuit 8 as a part of an interface signal for the interface 12.

A voltage-detected information signal 9 detected by the voltage detection circuit 8 is supplied to the reset circuit 10. The reset circuit 10 outputs a reset signal 11 in response to the voltage-detected information signal 9 as needed and supplies it to the interface/control circuit 4.

Further, the microcomputer 5 and the flash memory 6 are electrically connected to the interface/control circuit 4.

The microcomputer 5 is activated so as to control the entire circuits of the I/O card 1 and control the writing and reading of memory data between the personal computer 2 and the flash memory 6 of the I/O card 1.

Described specifically, the voltage detection circuit 8 detects the voltage of the source voltage signal 7 and outputs a 2V detected signal 9a or a 4.5V detected signal 9b, followed by application to the reset circuit 10.

Fig. 2 is a specific circuit diagram of the reset circuit 10. In Fig. 2, the reset circuit 10 is specifically composed of flip-flops 10a and 10b, a NAND circuit 10c and an OR circuit 10d. The 2V detected signal 9a outputted from the voltage detection circuit 8 is supplied to the OR circuit 10d of the reset circuit 10.

Further, the 4.5V detected signal 9b outputted from the voltage detection circuit 8 is supplied to a data input of the flip-flop 10a of the reset circuit 10. Furthermore, a clock CLK is also supplied to each of the flip-flops 10a and 10b. The reset circuit 10 outputs a reset signal 11 from the output of the OR circuit 10d based on these signals and supplies it to the interface/control circuit 4.

Fig. 3 is a waveform chart for describing the operation of the personal-computer system according to the first embodiment.

When the I/O card 1 having a dual operating voltage is activated, a signal at a Vsense pin that exists in the interface 12, is first read from the personal computer 12 side. Next, an initial source voltage signal for the I/O card 1 is set to 5V and the I/O card 1 is firstly activated under 5V. Thereafter, the source voltage signal is changed to a low source voltage signal 3.3V and the I/O card 1 is activated under the low source voltage signal 3.3V.

The state of a change of the source voltage signal 7 from 5V to 3.3V is represented as shown in Fig. 3(a). The voltage detection circuit 8 outputs the voltage-detected information signal 9 as shown in Fig. 3(b) in response to the change in source voltage signal 7 shown in Fig. 3(a). Namely, the voltage detection circuit 8 outputs the 2V detected signal 9a and the 4.5V detected signal 9b in response to the change in source voltage signal 7. A waveform shown in Fig. 3(c) is created by the NAND 10c of the reset circuit 10 based on the voltage-detected signals 9a and 9b. Hence the reset signal 11 is outputted in the form of a signal shown in Fig. 3(d) so as to be supplied to the interface/control circuit 4.

Namely, the waveform of the reset signal 11 shown in Fig. 3(d) is rest between source voltage signals 0V and 2V applied upon initial operation. Next, the waveform of the reset signal 11 is reset again between 4.5V and 5V prior to the initial source voltage signal 5V. Thereafter, the waveform of the reset signal 11 is reset upon change of the source voltage signal from 5V to 3.3V.

According to the first embodiment, as described above, the I/O card 1 is provided with the voltage detection circuit 8 and the reset circuit 10. Further, the reset circuit 10 generates the reset signal 11 to be supplied to the circuits such as the interface/control circuit 4 of the I/O card 1, etc. Thus, when the source voltage signal 7 changes from 0V to the initial source voltage 5V and from the initial source voltage 5V to the low operating source voltage 3.3V as shown in Fig. 3, the I/O card 1 can be assuredly reset.

As a result,, an internal state of the I/O card 1 can be determined. Thus, since a CPU mounted in the personal computer 2 makes it unnecessary to cause the I/O card 1 to write an initial value into the register and other inner circuits provided within the I/O card 1 after the source voltage signal has been changed, the time required to initially set the CPU can be shortened and a processing burden imposed on the CPU can be reduced.

[Second embodiment]

In the first embodiment, the reset circuit has been used to stabilize the states of the register and the inner circuits provided within the I/O card in response to the change in source voltage signal. In the second embodiment, however, an I/O card 1A is realized which is capable of optimizing an interface with a personal computer and an operating frequency based on a source voltage signal and stabilizing its internal state based on a voltage-detected information signal 9 outputted from a voltage detection circuit 8.

The I/O card 1A is different in characteristic from the I/O card 1 according to the first embodiment in that a selector circuit 30 for taking in or capturing the voltage-detected information signal 9 outputted from the voltage detection circuit 8 and outputting a select signal 31 therefrom is provided. Further, an interface/control circuit 4 is characterized by comprising a 5.0V interface circuit 41, a 3.3V interface circuit 42, a 5.0V clock generation circuit 43, a 3.3V clock generation circuit 44 and an interrupt circuit 40.

Incidentally, the 5.0V clock generation circuit 43 includes a 5.0V oscillating vibrator 45. Further, the 3.3V clock generation circuit 44 also includes a 3.3V oscillating vibrator 46.

The select signal 31 outputted from the select circuit 30 is supplied to the 5.0V interface circuit 41, the 3.3V interface circuit 42, the 5.0V clock generation circuit 43, the 3.3V clock generation circuit 44 and the interrupt circuit 40 of the interface/control circuit 4. Further, the interrupt circuit 40 generates an interrupt signal 35 from the select signal 31 and supplies it to a microcomputer 5. The microcomputer 5 interrupts the interface/control circuit 4 while the interface circuits 41 and 42 and the clock generation circuits 43 and 44 are selected based on the select signal 31.

(Select circuit 30):

Fig. 5 is a view showing a specific circuit configuration of the select circuit 30. Referring to Fig. 5, a 2V detected signal 9a outputted from the voltage detection circuit 8 is supplied to an AND circuit 30b, whereas a 4.5V detected signal 9b outputted therefrom is supplied to an inverter 30a. The 4.5V detected signal 9b is outputted as a 5.0V circuit select signal 31b. A signal outputted from the inverter 30a is supplied to the AND circuit 30b from which an AND output signal is outputted as a 3.3V circuit select signal 31a.

(5.0V interface circuit 41 and 3.3V interface circuit 42):

Fig. 6 is a view illustrating specific circuit configurations of the 5.0V interface circuit 41 and the 3.3V inter-

face circuit 42. Referring to Fig. 6, the 5.0V interface circuit 41 and the 3.3V interface circuit 42 respectively include 5.0V input buffers 61 through 63, which amplify signals sent from the interface 12. Signals outputted from the 5.0V input buffers 61 through 63 are supplied to their corresponding selectors 81 through 83. Further, the 5.0V and 3.3V interface circuits 41 and 42 respectively include 3.3V input buffers 71 through 73, which receive the signals from the interface 12. Signals outputted from the 3.3V input buffers 71 through 73 are also supplied to their corresponding selectors 81 through 83.

The selectors 81 through 83 supply signals respectively selected based on the 3.3V circuit select signal 31a and the 5.0V circuit select signal 31b outputted from the selector circuit 30, to their corresponding inner circuits. (5.0V clock generation circuit 43 and 3.3V clock generation circuit 44):

Fig. 7 is a view showing specific circuit configurations of the 5.0V clock generation circuit 43 and the 3.3V clock generation circuit 44. Referring to Fig. 7, a 5.0V oscillation circuit 64 oscillates in a predetermined frequency using a 5.0V oscillating vibrator 45, an inverter 64a, a resistor 64b and capacitors 64c and 64d. An oscillated signal is supplied to a selector 84.

Further, a 3.3V oscillation circuit 74 oscillates in a predetermined frequency using a 3.3V oscillating vibrator 46, an inverter 74a, a resistor 74b and capacitors 74c and 74d. An oscillated signal is supplied to the selector 84.

In response to the 3.3V circuit select signal 31a and the 5.0V circuit select signal 31b outputted from the select circuit 30, the selector 84 outputs either one of the oscillated signals to its corresponding inner circuit as a system clock.

Fig. 8 is a waveform chart for describing the operation of the personal computer according to the second embodiment. Referring to Fig. 8, a waveform chart of Fig. 8(a) for describing variations in source voltage signal 7 and a waveform chart shown in Fig. 8(b), of the voltage-detected information signal 9 are similar to those shown in Figs. 3(a) and 3(b) of Fig. 3. The select circuit 30 generates the 5.0V circuit select signal 31b shown in Fig. 8(c) and the 3.3V circuit select signal 31a shown in Fig. 8(d) in response to the voltage-detected information signal 9 shown in Fig. 8(b) and supplies them to the interface/control circuit 4.

The 5.0V input and the 5.0V oscillated-signal output or the 3.3V input and the 3.3V oscillated-signal output are selected by the selector 81 through 83 of the 5.0V and 3.3V interface circuits 41 and 42 supplied with the 5.0V circuit select signal 31b shown in Fig. 8(c) and the 3.3V circuit select signal 31a shown in Fig. 8(d) and the selectors 84 of the 5.0V and 3.3V clock generation circuits 43 and 44 supplied with the 5.0V circuit select signal 31b and the 3.3V circuit select signal 31a.

In the second embodiment, the 3.3V input and the 3.3V oscillated-signal output are selected when the source voltage signal 7 ranges between 2V and 4.5V. When the source voltage signal 7 is more than or equal to 4.5V, the 5.0V input and the 5.0V oscillated-signal output are selected.

(Effects of second embodiment):

The second embodiment described above can bring about advantageous effects that since the select circuit 30 is provided within the I/O card 1A, the input interface and clock generation optimal to the source voltage signal 7 can be carried out by generating the select signals 32 and 33 using the voltage-detected information signal 9 detected and produced by the voltage detection circuit 8 in response to the voltage variation in source voltage signal 7.

Accordingly, the state of the inner circuits in the I/O card 1A can be stabilized and determined even if the source voltage signal varies.

Therefore, the internal state of the I/O card 1A can be determined. Thus, since the CPU provided within the personal computer 2 makes it unnecessary to allow the I/O card 1A to write the initial value into the register and other inner circuits provided within the I/O card 1A after the change in source voltage signal, an initialization time of the CPU can be shortened and a processing burden imposed on the CPU can be reduced.

In the aforementioned embodiments, 5.0V and 3.3V have been used as the source voltage signal. As an alternative, however, other source voltage signal may be applied by varying the level of a detected voltage.

Further, the aforementioned second embodiment describes the case where the input of the interface circuit is used as an example. However, the output of the interface circuit may be applied if the same select signal is used.

Furthermore, the aforementioned embodiments describe the case where the personal computer 2 is used as a host device. However, other various devices may be adopted as the host device. As the host device, may be mentioned those such as an information processor, a measuring device, a storage device, a display unit, a printer device, etc.

Still further, any one of a serial interface, a parallel interface, etc. can be applied between the host device and the I/O card or IC memory card.

Still further, various devices such as a disk card, a RAM card, a ROM card, an arithmetic card, a modem card, a cassette device, a board, a module, a unit (such as a harddisk unit), etc. can be adopted as objective devices to be connected as well as the I/O card and the IC memory card.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art on reference to this description.

Claims

1. An internal state determining apparatus comprising:
at least one inner circuit;
detecting means for detecting a change in voltage supplied from an external device and outputting a detected signal in response to the change in voltage; and
internal state determining means for determining said inner circuit so as to fall into a predetermined state in response to the detected signal.

2. An internal state determining apparatus according to claim 1, wherein said detecting means selectively receives first and second voltages from the external device and outputs first and second detected signals in response to the first and second voltages and said internal state determining apparatus detects that the second voltage has been received after the receipt of the first voltage and determines said inner circuit so as to fall into the predetermined state.

3. An internal state determining apparatus according to claim 2, which detects that the second voltage has been received after the receipt of the first voltage and outputs a reset signal for determining said inner circuit into an initial state to said inner circuits.

4. An internal state determining apparatus comprising:
a plurality of inner circuits;
detecting means for detecting a change in voltage supplied from an external device and outputting a detected signal in response to the change in voltage;
a plurality of clock generators for generating clocks different from one another;
a plurality of interface circuits for receiving a signal inputted from the outside and respectively supplying internal signals to said plurality of inner circuits; and
internal state determining means for selecting any one of said plurality of clock generators and any one of said plurality of interface circuits in response to the detected signal and determining each of said plurality of inner circuits so as to fall into a predetermined state.

5. An internal state determining apparatus according to claim 4, wherein said detecting means selectively receives first and second voltages from the external device and outputs first and second detected signals in response to the first and second voltages, and said internal state determining apparatus detects that the second voltage has been received after the receipt of the first voltage, changes one of said plurality of clock generators to the other one of said plurality of clock generators and switches one of said plurality of interface circuits to the other one of said plurality of interface circuits, thereby determining said each inner circuit so as to fall into the predetermined state.

FIG.1

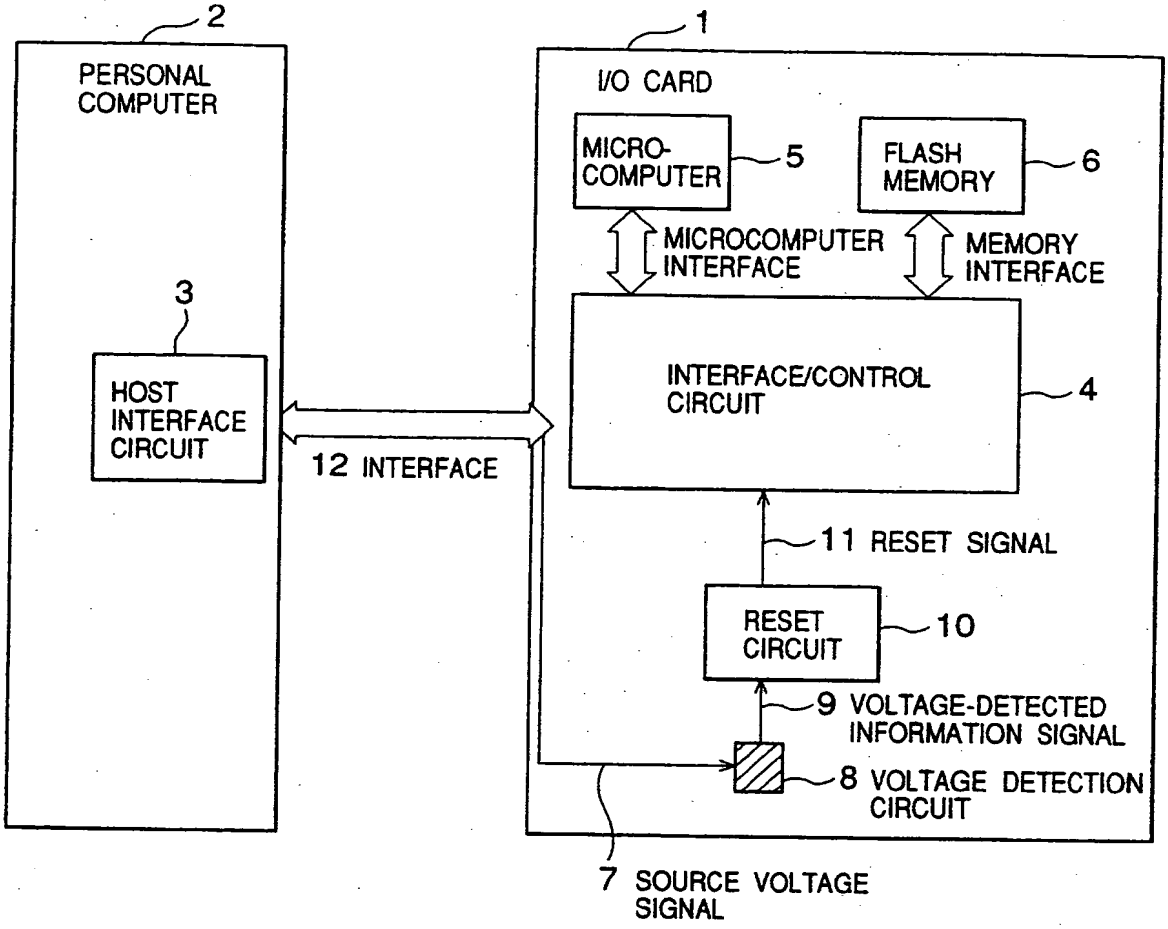
2
PERSONAL COMPUTER
3
HOST INTERFACE CIRCUIT
12 INTERFACE
1
I/O CARD
MICRO-COMPUTER
5
FLASH MEMORY
6
MICROCOMPUTER INTERFACE
MEMORY INTERFACE
INTERFACE/CONTROL CIRCUIT
4
11 RESET SIGNAL
RESET CIRCUIT
10
9 VOLTAGE-DETECTED INFORMATION SIGNAL
8 VOLTAGE DETECTION CIRCUIT
7 SOURCE VOLTAGE SIGNAL

FIG.2

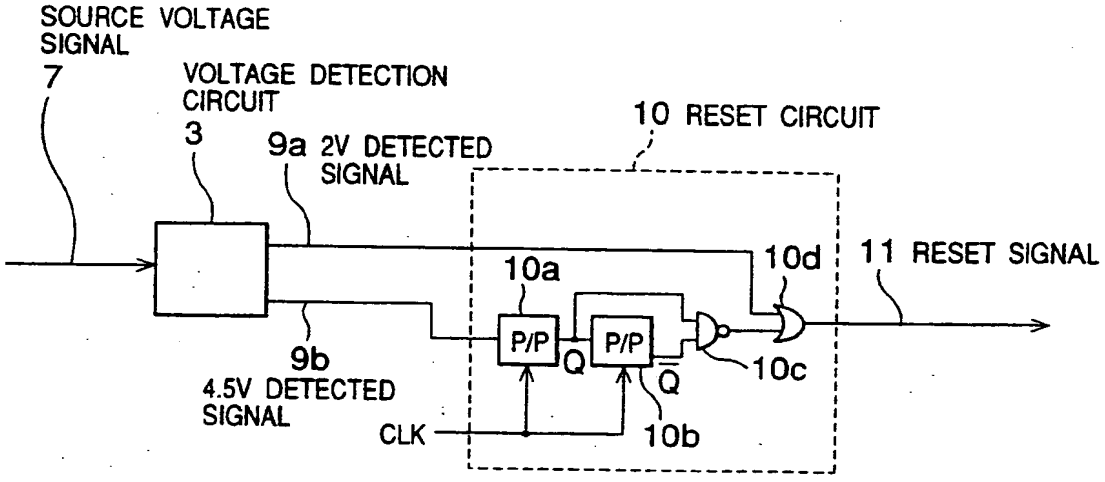
SOURCE VOLTAGE SIGNAL
7
VOLTAGE DETECTION CIRCUIT
3
9a 2V DETECTED SIGNAL
10 RESET CIRCUIT
10a
10d
11 RESET SIGNAL
P/P
Q
P/P
$\bar{Q}$
10c
9b
4.5V DETECTED SIGNAL
CLK
10b

FIG.3

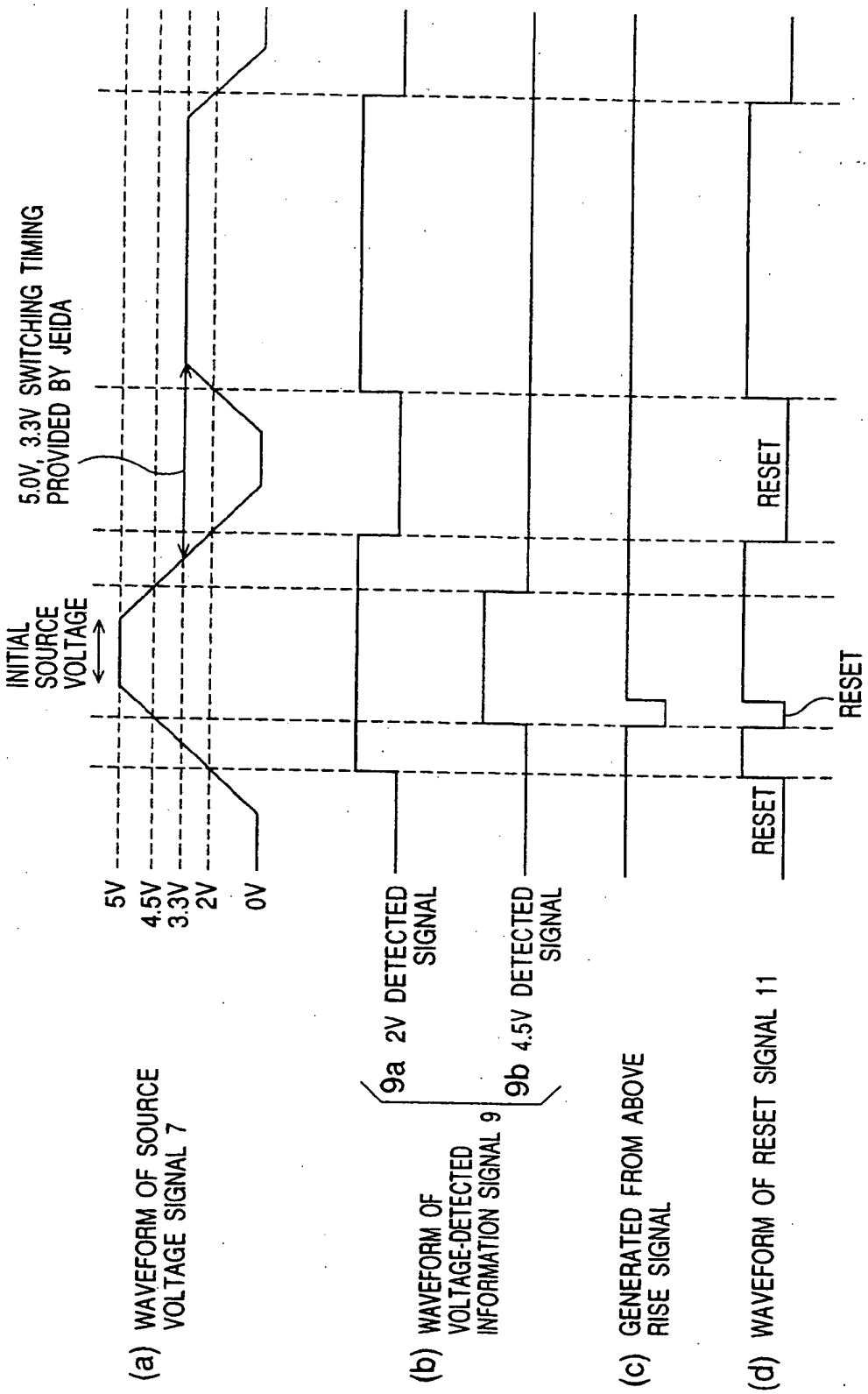

FIG.4

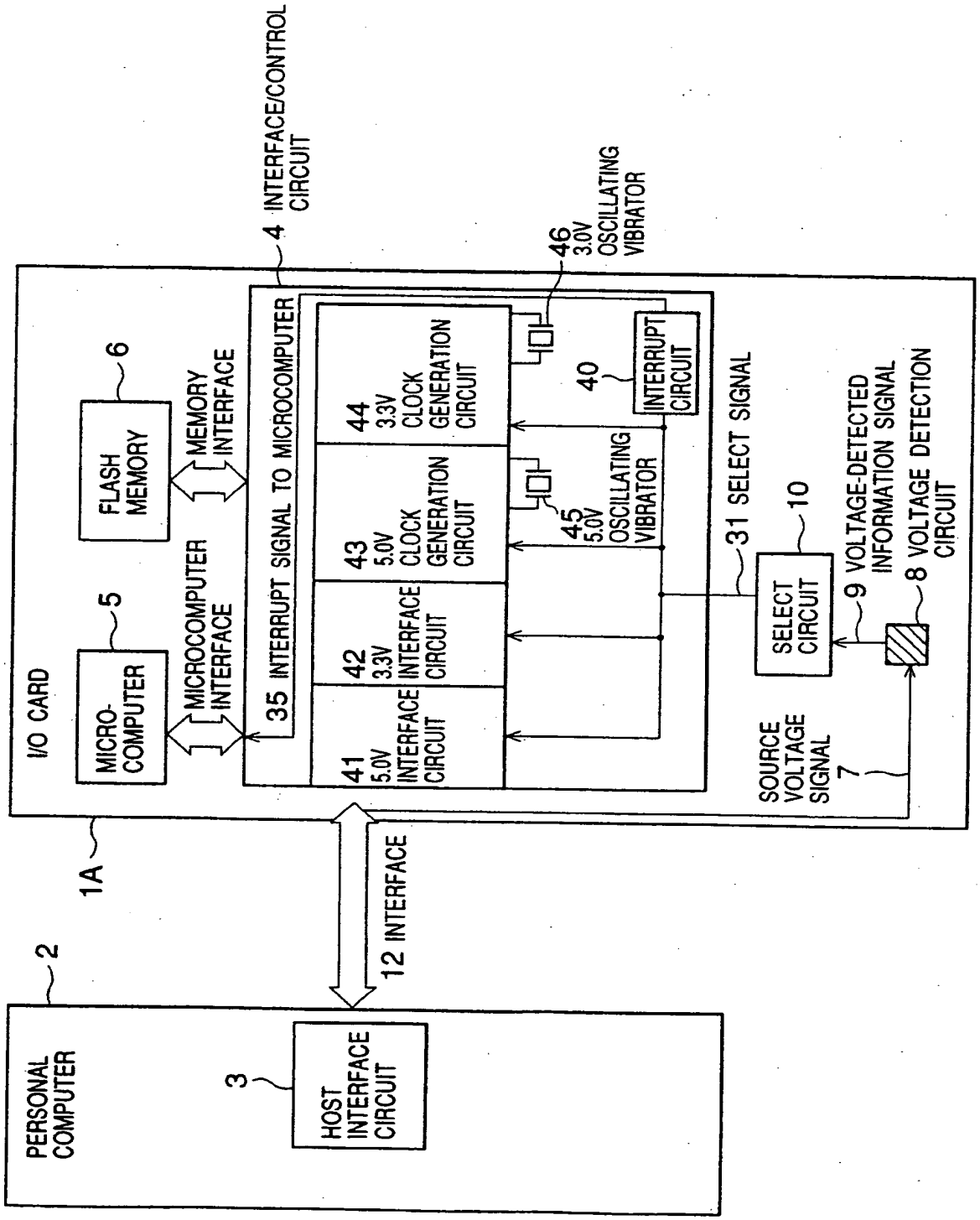
PERSONAL COMPUTER
2
HOST INTERFACE CIRCUIT
3
12 INTERFACE
1A
I/O CARD
MICRO-COMPUTER
5
MICROCOMPUTER INTERFACE
FLASH MEMORY
6
MEMORY INTERFACE
4 INTERFACE/CONTROL CIRCUIT
35 INTERRUPT SIGNAL TO MICROCOMPUTER
41 5.0V INTERFACE CIRCUIT
42 3.3V INTERFACE CIRCUIT
43 5.0V CLOCK GENERATION CIRCUIT
44 3.3V CLOCK GENERATION CIRCUIT
45 5.0V OSCILLATING VIBRATOR
46 3.0V OSCILLATING VIBRATOR
40 INTERRUPT CIRCUIT
31 SELECT SIGNAL
SELECT CIRCUIT
10
9 VOLTAGE-DETECTED INFORMATION SIGNAL
8 VOLTAGE DETECTION CIRCUIT
SOURCE VOLTAGE SIGNAL
7

FIG.5

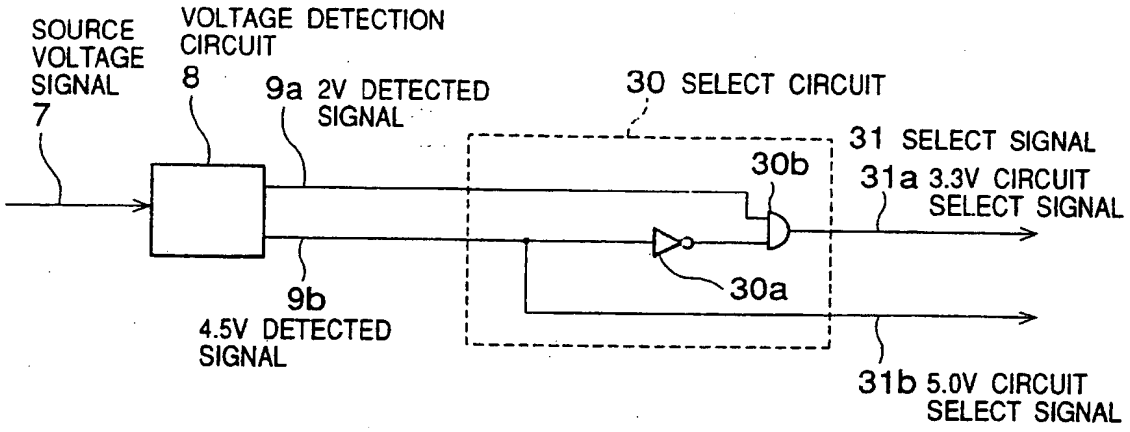

FIG.6

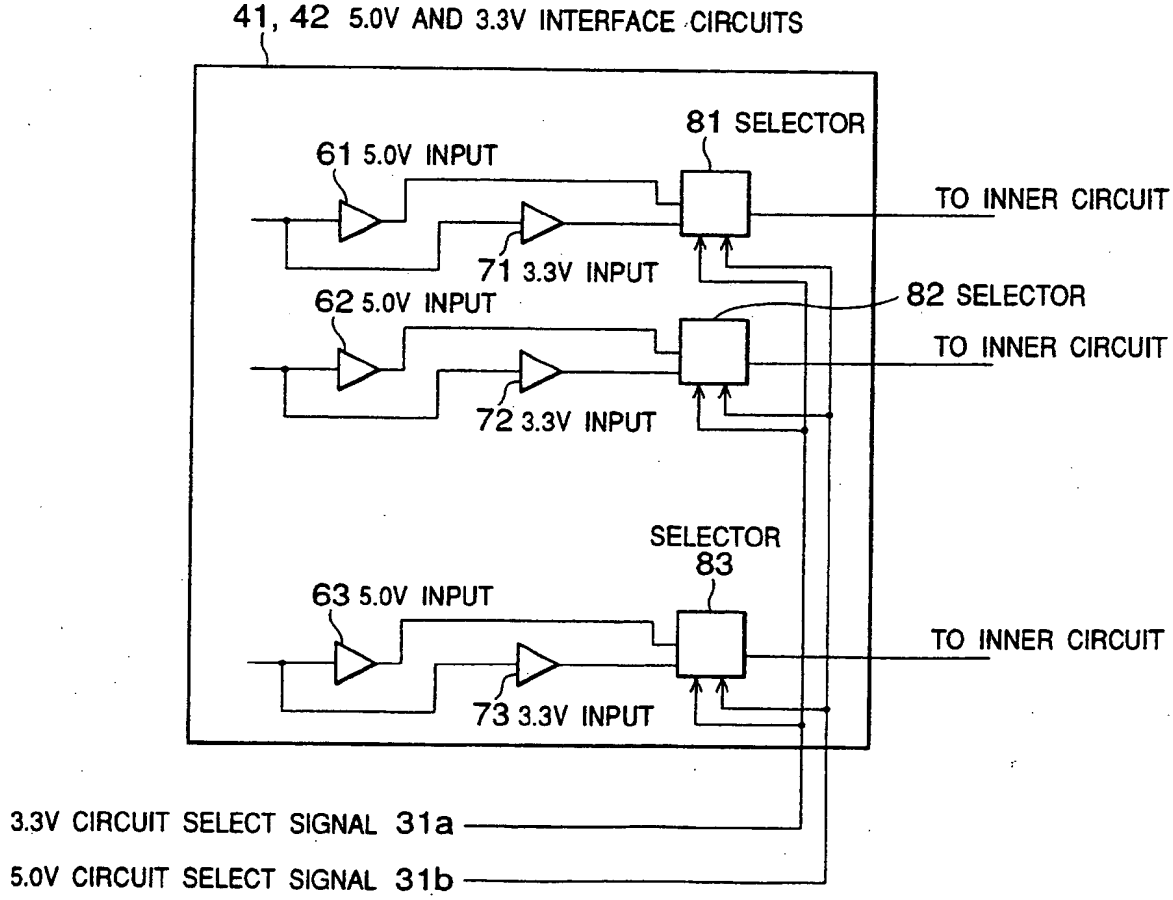

FIG.7

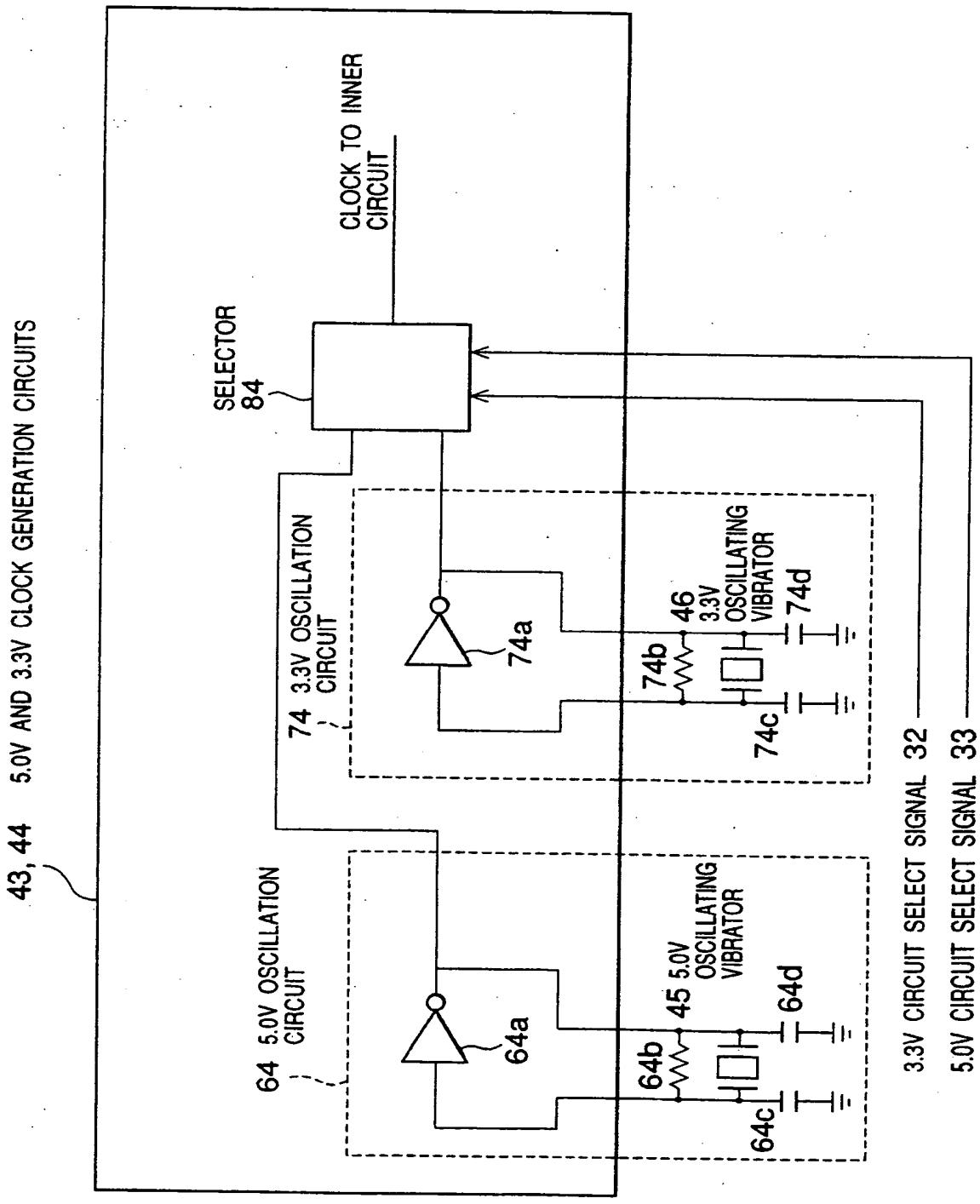

FIG.8